Form PTO-1449	Docket Number (Optional)	Application Number
INFORMATION DISCLOSURE CITATION IN AN APPLICATION (Use several sheets if necessary)	4720US (00-1120)	09/943,968
	Applicant **Leonard Forbes**	
	Filing Date **August 30, 2001**	Group Art Unit **2631**

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

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FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

DH		K. Yip, "Clock tree distribution: balance is essential for a deep-submicron ASIC design to flourish," IEEE Potentials, Vol. 16, no. 2, pp 11-14, April-May 1997.
DH		K. M. Carrig et al., "A Clock methodology for high-performance microprocessors," Proc. Custom Integrated Circuits Conference, Santa Clara, CA, May 5-8, pp. 119-122, 1997.
DH		J. L. Neves et al., "Automated synthesis of skew-based clock distribution networks," VLSI Design, Vol. 7, no.1, pp. 31-57, 1998.
DH		T. Meincke et al., "Globally asynchronous locally synchronous architecture for large high-performance ASICs," IEEE Symp. on Circuits and Systems, Orlando, FL, 30 May-2 June, Vol. 2, pp. 512-515, 1999.

EXAMINER	DATE CONSIDERED
	12/09/04

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.